REMARKS

In response to the Office Action mailed October 23, 2006, Applicants respectfully request reconsideration of the Application in view of the foregoing Amendments and the following Remarks. The claims as now presented are believed to be in allowable condition.

Claims 1 and 11 have been amended. Claims 1-20 remain in this application, of which claims 1 and 11 are independent claims.

Amendment to Specification

Note that the "Technical Field" of the Present Application has been amended to better reflect the recitation of the claims which are directed to testing of a memory device, and more particularly, to cycling through addresses of a flash memory device with minimized charge gain failure during testing of the flash memory device.

Rejection of Claims 1-5, 7-9, 11-15, and 17-19 under 35 U.S.C. §103(a)

Claims 1-5, 7-9, 11-15, and 17-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,883,844 to So (hereafter referred to as "So") in view of U.S. Patent No. 6,308,249 to Okazawa (hereafter referred to as "Okazawa"). Applicants respectfully traverse this rejection.

The rejection of claims 1 and 11 under 35 U.S.C. §103(a) as being unpatentable over So in view of Okazawa is not appropriate because claims 1 and 11 have been amended, and a prima facie case of obviousness cannot be established for such amended claims.

In giving an obviousness rejection, the Examiner bears the initial burden of factually supporting a prima facie conclusion of obviousness. (See, MPEP, §2142). To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be ***some suggestion***

or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, ***the prior art references*** must teach or suggest ***all the claim limitations***. (See, MPEP, §2142.) (Emphasis added.)

The rejection of amended claims 1 and 11 under 35 U.S.C. §103(a) as being unpatentable over So in view of Okazawa is not appropriate because *inter alia* these prior art references fail to teach or suggest all the claim limitations and because there is no motivation or suggestion in these references to combine or modify these references to the present invention.

Amended claims 1 and 11 recite that the predetermined number of bits for each address includes row and column address bits with each of ***all possible row and column addresses*** of the row and column address bits being cycled through for the application of the stressing signals.

For example, the Present Application at page 6, line 20 to page 7, line 2 describes address bits A[20:0] including row address bits A[15:7] and column address bits A[6:0]. In addition, the Present Application clearly describes cycling through all possible addresses with the address bits A[20:0] including cycling through all possible row and column addresses.

In contrast, So clearly teaches away from such a limitation by repeatedly touting testing only a extremely small portion of the memory block for reducing test time as stated at col. 1, line 66 to col. 2, line 67 of So:

> ....Some conventional parallel test operations can continue to take ***extensive amounts of time*** to accomplish the testing results.
>
> ....
>
> ....A method preferably includes generating a high frequency waveform signal and generating a test pattern across boundaries ***between only two columns and only two rows*** of the memory block, i.e., preferably adjacent columns and adjacent rows, responsive to the high frequency waveform signal so as to determine whether to accept or reject the memory block. (Emphasis Added.)

Repeatedly, col. 5, lines 3-27 of So states:

> ....for selectively stress testing ***only portions of the memory block*** 20 and not other portions for a concentrated predetermined period of time so as to determine to whether to accept or reject the memory block 20...
>
> ....***only selected potentially weak areas of a memory block*** need be tested to thereby statistically predict whether to accept or reject the memory block 20 based upon the results of the test. These selected areas, for example, are preferably weak areas across boundary lines preferably between side-by-side columns and/or side-by-side rows. (Emphasis Added.)

Thus, the main purpose of So is to test only a very small portion (only two rows and two columns) of the memory block for minimizing test time. Generally, one of ordinary skill in the art knows that a whole "memory block" is comprised of all possible addresses of the row and column address bits.

So repeatedly touts minimizing test time by stressing and testing only a very small portion of the memory block (such as two rows and two columns when a memory block typically has tens of thousands of row and columns).

Thus, So ***strongly teaches away*** from the limitation of cycling through each of ***all possible*** row and column addresses of the row and column address bits for the application of the stressing signals, as recited in amended claims 1 and 11.

Okazawa simply discloses typical read/write access of a memory device within a general computer system using gray code address sequencing for minimizing power consumption. Okazawa no where even remotely mentions any stress testing of any memory device.

In addition, for typical read/write access of the memory device in the general computer system of Okazawa, just the selected row and column addresses of the memory device associated with data to be processed would be sequenced. Thus, all possible row and column addresses of

the memory device would be not cycled through for typical read and write accessing of the memory device in Okazawa.

Thus, So and/or Okazawa, either individually or in combination do not disclose, teach, or suggest cycling through each of ***all possible*** row and column addresses of the row and column address bits for the application of the stressing signals. In fact, So repeatedly and strongly teaches away from such a limitation by touting minimization of test time by stressing and testing only a very small portion of the memory block.

Accordingly, a prima facie conclusion of obviousness of claims 1 and 11 cannot be established because So and/or Okazawa fail to suggest or motivate all the claim limitations of claims 1 and 11, and the rejection of claims 1 and 11 under 35 U.S.C. §103(a) should be withdrawn.

Claims 2-5 and 7-9, which depend from and further limit claim 1, are allowable for at least the same reasons that claim 1 is allowable as stated above.

Claims 12-15 and 17-19, which depend from and further limit claim 11, are allowable for at least the same reasons that claim 11 is allowable as stated above.

Okazawa is Nonanalogous Art

The MPEP at §2141.01(a)I states:

> I. TO RELY ON A REFERENCE UNDER 35 U.S.C. 103, IT MUST BE ANALOGOUS PRIOR ART
>
> ....In order to rely on a reference as a basis of rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned....
>
> ....A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem.

Note that the Technical Field of the Present Application has been amended to better reflect the Present Invention as recited by the current pending claims to be directed to ***testing*** of a memory device, and more particularly, to cycling through addresses of a flash memory device with minimized charge gain failure during testing of the flash memory device.

In contrast, Okazawa is just directed to typical read/write access of a memory device within a general computer system and is in no way even remotely directed to any testing of a memory device. Thus, Okazawa is in a different field of endeavor from the Present Invention as recited in the claims which is directed to ***testing*** of a memory device.

In addition, Okazawa is directed to accessing the memory device using gray code sequencing for minimizing power consumption when the memory device is accessed continuously by the main processor of during the 3-5 year life-time of a typical computer system. Okazawa for each access of the memory device would sequence through addresses of just a small portion of the memory device associated with a read/write operation.

Generally, charge gain failure is not likely to occur if all possible row and column addresses of the row and column address bits are not cycled through for the application of the stressing signals. Thus, Okazawa is in no way directed to using Gray code sequence for the typical read/write access of the memory device for minimizing charge gain failure.

In summary, because Okazawa is not in the field of applicant's endeavor and is not reasonably pertinent to the particular problem with which the Present Invention is concerned, Okazawa is nonanalogous prior art.

Rejection of Claims 6, 10, 16, and 20 under 35 U.S.C. §103(a)

Claims 6 and 10, which depend from and further limit claim 1, are allowable for at least the same reasons that claim 1 is allowable as stated above.

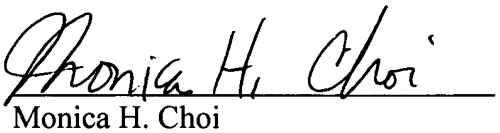
Claims 16 and 20, which depend from and further limit claim 11, are allowable for at least the same reasons that claim 11 is allowable as stated above.

Conclusions

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. Please feel free to contact the undersigned should any questions arise with respect to this case that may be addressed by telephone.

Respectfully submitted,
for the Applicant(s)

Dated: January 9, 2007

By: 

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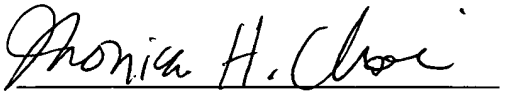
CERTIFICATE OF MAILING

The undersigned hereby certifies that the foregoing AMENDMENT AND RESPONSE AS SUBMISSION FOR RCE is being deposited in the United States Postal Service, as first class mail, postage prepaid, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 9th day of January, 2007.



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